ULTRAFAST HIGH POWER SWITCHING DIODES

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ABSTRACT

Impressive progress in semiconductor switch technology has been demonstrated at the A. I. Ioffe Physiotechnical Institute in St. Petersburg, Russia, by Grekhov, Kardo-Sysoev and colleagues. In general, the Ioffe group's technology demonstrates faster switching at higher voltages and peak powers (from the moderate current, sub-nanosecond time scale to the microsecond time scale at multiple kilo Ampere currents) than existing commercial devices. In the moderate voltage (1 KV), moderate current (100 A) regime, the Ioffe group's technology demonstrates switching times of 2 ns or a *di/dt* of 5 x 10^{10} A/s. In the thyristor area, large diameter devices have demonstrated rates of current rise approaching 10^{12} A/s, which is comparable with spark gaps. In addition, the ultrafast (50 ps), high voltage (15 KV) pulse rise times demonstrated by Grekhov and colleagues surpasses the switching speed produced by nonlinear GaAs switches in the United States.

A three year research project is underway in collaboration with the Ioffe group (led by Dr. Kardo-Sysoev) which seeks to define the physics, assess the technology, and identify the critical parameters that allow for successful development of semiconductor switches capable of operating at the parameters described above. The initial stage of the program studies individual switches produced by the Ioffe group in order to verify their operational parameters. The second stage of the program will study the physics issues important in achieving the operational specifications. The final stage of the program will suggest modifications to the device manufacture process that may yield further improvements in performance.

This paper presents information on a computer-controlled test stand that was developed for testing a variety of components produced by the Ioffe group. Information on circuit modeling using PSPICE and one specific test circuit are discussed. Finally, performance results for two kinds of Drift Step Recovery Diodes (DSRD) are presented.

Experiment Overview and Computer Control

Pulse generation using the DSRD requires switching two sides of an inductive-capacitive storage circuit at the appropriate times with a certain degree of accuracy and exploiting the turn-off behavior of the device. Two types of DSRDs are tested in this experiment and are classified as either "slow" or "fast" switching. The specified turn-off times for the "slow," or Type I, and "fast," or Type II, switching DSRD are 2-5 ns and 0.5-1.5 ns, respectively. A block diagram of the experimental set-up is shown in Fig. 1. It is desirable to have the experiment computer controlled for ease of operation and unattended lifetime testing. At the heart of the system is a 486DX-66 computer. The computer is equipped with a National Instruments General Purpose Interface Bus (GPIB) board and a PC-LPM-16 Analog/Digital I/O interface board.

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A graphical programming software, LabVIEW,[1] is used to create a Virtual Instrument (VI) to control the interface boards and the experiment. The GPIB interface is used in conjunction with the VI for waveform monitoring, information storage, and pulse parameter detection in lifetime testing. The I/O interface board controls firing of the circuit under test by providing a trigger to the HP 8015A pulse generator. The VI controls all aspects of the circuit, such as single shot or continuous operation mode, frequency of firing in continuous mode, number of pulses, output pulse parameter detection, and storage of output pulse waveforms as desired. Although forced air cooling of the circuit under test is provided, a thermal shutdown was also incorporated to protect the MOSFETs in the circuit. The thermal shutdown safety feature was implemented by sensing the temperature at the MOSFET-to-heatsink interfaces using Fluke 80TK thermocouple modules. The output of the modules, which is 1 mV per degree (C or F selectable), are fed into an analog input of the I/O board and conversion of volts to degrees takes place within the VI. A front panel readout of temperature is also available.

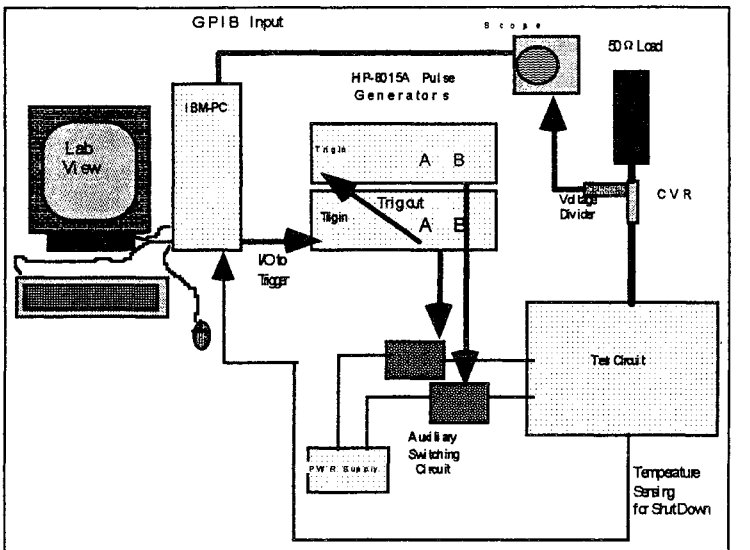

Figure 1. Block diagram of experimental set-up.

During the initial design phase of the project, it was proposed that the circuit be directly controlled from the computer. It was found that the I/O board could not provide enough gate voltage to directly drive the main MOSFETs. An auxiliary switching circuit using two more MOSFETs, a voltage divider network and a dual variable power supply was devised to provide the required gate voltage. It was also found that the I/O board's output impedance prohibited fast switching of the auxiliary MOSFETs and the board's clock frequency (1 MHz) would not allow generation of the required delay between the two control pulses (100-300 ns). Two HP 8015A pulse generators had to be used to obtain the required drive pulses and delay on the second pulse. Since the source of the second MOSFET is not referenced to the common ground, the second pulse generator had to be isolated from the rest of the circuit. This was accomplished by installing a 1:1 transformer for the trigger input and isolating the chassis ground.

In summary, the VI is controlled by point and click operations with the mouse via the front panel. The VI controls the I/O board to provide a trigger to pulse generator one (PG1). The output trigger of the first pulse generator triggers the second (PG2) through inductive coupling. The pulse generators provide complimentary pulses with the appropriate delay of the second pulse to turn off the auxiliary switches. "Turn-off" of the auxiliary switches allows a rising voltage on the gate of the main switches which then turn on. The L-C storage circuits first forward-bias and then reverse-bias the DSRD. When timed appropriately, the DSRD will open circuit and produce a voltage pulse at the output. The output voltage is monitored on an oscilloscope and displayed on the VI front panel by using the GPIB interface. (Output current can also be measured but is not displayed on the VI front panel.)

PSPICE Modeling

PSPICE modeling of the circuit is straightforward for all components except the DSRD. The large-signal model for the diode allows for charge storage effects of the device but only if the appropriate parameters are specified in the .MODEL statement for the diode. The parameters that must be specified in the .MODEL statement are: CJO, zero-bias junction capacitance; M, grading coefficient; VJ, junction potential; FC, the coefficient for the forward-bias depletion capacitance formula; and TT, transit time.

The zero-bias junction capacitance for a Type I and Type II DSRD were measured and found to be 1050 pF and 82 pF, respectively. M was set at 0.5 for an abrupt junction. The junction potential for the Type I and Type II DSRDs were measured at 0.765 V and 2.09 V, respectively. The coefficient for forward-bias depletion calculation was left at the default value of 0.5. The transit time was set at 2.5 μs for both the Type I and Type II DSRDs based on initial descriptions of circuit operation.

Circuit Description and Component Selection

The schematic of the test circuit is shown in Fig. 2. In anticipation of significant heat dissipation from the main switching MOSFETs, the circuit was constructed on a large aluminum heat sink and forced air cooling was provided. The auxiliary switching circuits were constructed in separate heat sinked and shielded boxes to prevent any interference from the main circuit. Large "doorknob" type ceramic capacitors were used for initial charge storage because of their high breakdown voltage. Thin copper strips were used for interconnection. To minimize stray inductance and reduce unwanted resistance, component layout was kept as compact as possible. A type HN connector was used at the output in anticipation of generating pulses of 10 kV amplitude.

It can be seen from Fig. 2 that there are two separate legs to the circuit. The output voltage of the available pulse generators (HP 8015A) was only 8 volts into 50 Ω. This voltage is insufficient to fully enhance the channels of the main MOSFETs. To achieve the required gate drive voltage, an auxiliary drive circuit was constructed. The auxiliary MOSFETs merely act as turn-off devices and allow the gates of the main MOSFETs to go to half the auxiliary supply voltage through a voltage divider network. To prevent any unwanted ringing in the trigger circuit, Caddock MP850 series non-inductive power resistors [2] were utilized. These resistors offer far lower inductance than wire wound power resistors.

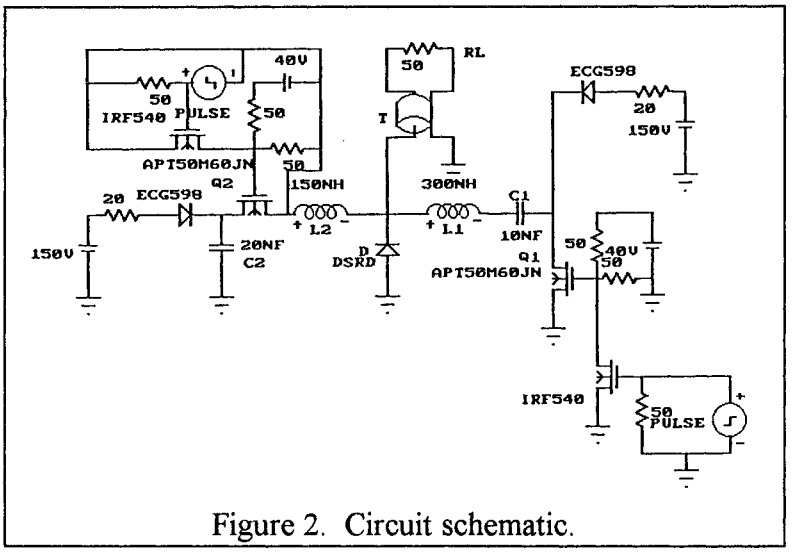

Figure 2. Circuit schematic.

The main MOSFETs are Advanced Power Technologies APT50M60JN.[3] These MOSFETs were chosen for their breakdown voltage (500 V), current handling capability (71 A continuous, 284 A pulsed), fast switching (t_r = 30 ns) and low "on" resistance (0.06 Ω). For initial circuit design only one MOSFET per leg is needed. Auxiliary MOSFETs are Internal Rectifier's IRF-540s. These MOSFETs were chosen for availability and switching speed. Originally, IRF-610s were used for the auxiliary switch. The rise time of the IRF-610 was about half that of the main switch and appeared to cause distortion of the first half cycle of current flow in the circuit legs.

The circuit operation is described as follows. Initially, capacitors C_1 and C_2 are charged to the supply voltage through a current limiting resistor and blocking diodes. The current path to charge C_1 is through the load resistor, R_L. The value of the current limiting resistor must be chosen so that the limiting capacitor, C_1, can be charged in a time less than the minimum anticipated period. For this circuit the maximum expected operating frequency is 100 kHz which gives a period of 10 μs. The rise time of the output pulse is determined by the switching characteristics of the diode. The fall time of the pulse is determined by the inductive decay constant, $\tau_L = L/R_L$, and inductor size is chosen based on the desired fall time. Keeping in mind that the load resistor will see two inductors in parallel, the size of the inductors must be doubled for the desired τ_L. To match the expected turn-off time of the Type I DSRD, τ_L was set at 3 ns. With R_L = 50 Ω, this gives 300 nH for L_1 and L_2. The inductors are fabricated using 16 gauge enameled copper wire. Ten turns were tightly wound around an 8 mm diameter core yielding an inductance of about 300 nH.

The value of the capacitors were chosen based on a desired resonant frequency of 15.71 Mrad/sec giving a corresponding period of the resonant circuit T=400 ns. In practice, the period may be varied from 200-600 ns. A standard value of 10 nF was initially chosen for C_1 and C_2.

Pulse generation takes place by exploiting the reverse biased switching characteristics of the diode, as shown in Fig. 3. During forward current flow through the diode, charge will be stored in the device in both the depletion region capacitance and by the minority carriers injected into the bulk regions. Under reverse biased conditions a large initial current is allowed to flow until the stored charge in the device is depleted. The reverse recovery time, t_{rr}, is split into two components: the stored charge depletion time, t_s, and the switching time, t_r. When the stored charge is depleted, the diode switches from the high conductance "on" state to a low conductance "off" state in a time t_r. The switching time t_r is controlled primarily by the recombination of minority carriers in the crystal material. If t_r is much less than t_s the transition is characterized as abrupt.[4] This will be the case for the DSRDs used in this experiment. Ideally the diode switches in zero time.

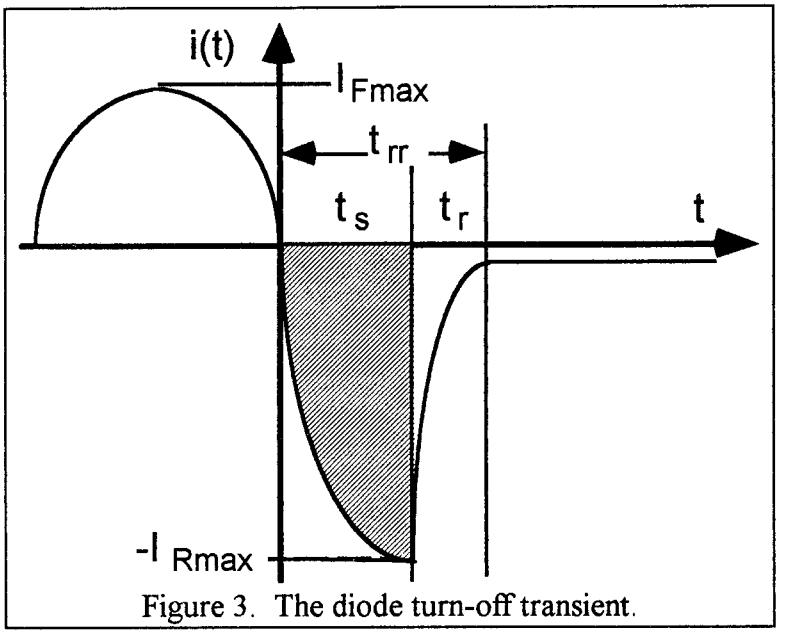

Figure 3. The diode turn-off transient.

Operation is initiated by closing switch Q_1 (Fig. 2). This allows forward current flow through the DSRD and causes charge storage. Switch Q_2 is closed at the point when reverse current starts to flow through the diode. In theory, we should be able to get the same amount of current in the first half cycle of the second leg as we did in the first half cycle of the first leg. In actuality this may not always be the case and will depend on the circuit quality factor, Q. As reverse current flows through the DSRD, stored charge is removed. If the reverse current is twice that of the forward, the stored charge will be removed in T/4 and the diode will switch off at the point of maximum current flow through the device.

For a Type I DSRD the stated turn off time is 2-5 ns. If, for example, the turn off time is 3 ns and 100 Amps were passing through the DSRD at turn off, the rate of change of current, *di/dt*, would be 3.33×10^{10} A/s. The *di/dt* in each leg of the circuit would be changing at half this rate, or 1.67×10^{10} A/s. For the given inductance this would give a voltage across L_1 and L_2 equal to 2.5 KV at the instant of switching.

In reality, the current flow and Q in the two sides of the actual circuit were not equal and some modifications were required. The final component values used are shown in Fig. 2. In addition, stray inductance in the circuit wiring and components made the period a little longer than expected. It was desired to have the period of both sides of the circuit be about the same, but with less current in the first side. Since the second side had the lower Q value, L_2 and C_2 were fixed at five turns and 20 nF, respectively. This provided a period of about 360 ns. To lower the current in the first side while keeping the same period, L_1 and C_1 were made 10 turns and 10 nF, respectively. With these component values the reverse current flow through the DSRD (I_R) could now be made more than twice the forward current flow (I_F). Current flow in the first leg of the circuit could also be adjusted by varying the auxiliary supply voltage to the gate of the main MOSFET.

The desired output pulse voltage can now be set by simply varying the supply voltage being careful not to exceed any component limitations. For this circuit the limitation is determined by the MOSFET maximum V_{DS} (500 V) and the DSRD breakdown voltage (2.5 KV).

Experimental Data

Output voltage pulses into a 50 Ω load are shown below in Figs. 4 and 5 for a Type I and Type II 2.5 KV breakdown voltage DSRD, respectively. Stated rise times are from 10% to 90% of the maximum amplitude, labeled "c" in the figures.

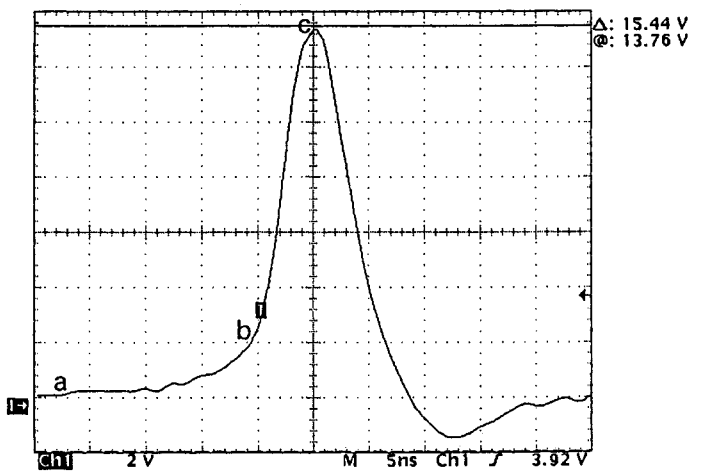

Figure 4. Slow DSRD output pulse (1V=143.2V at output). The time scale is 5 ns/div.

The specified t_r of the Type I DSRD is 2 to 5 ns. Figure 4 shows a slowly ramping portion from "a" to "b" before a rapid transition phase from "b" to "c." This slow ramping period is a function of device parameters and initial charge storage. Both the slow ramping period and the rise time are affected by the initial charge stored in the device.[5] In general, the length and peak voltage of the slow ramping period and the rise time of the waveform will increase with increasing stored charge in the device.

The load current and voltage were monitored using a T&M Research Products series VL current viewing resistor (CVR) with a voltage divider, and sampled using a Tektronix TDS-350 oscilloscope. All coaxial lines were properly terminated. Since the CVR, voltage divider, and oscilloscope all have finite and nonzero rise times an error will be introduced in the measured rise time, t_M. The specified nominal rise times for the CVR and voltage divider are 0.3 ns and 3.0 ns, respectively. The specified nominal rise time of the TDS-350 is 1.5 ns. It can be shown that the measured rise time is given by:[6]

$$t_M = (t_P^2 + t_{CVR}^2 + t_I^2)^{0.5} \quad (1)$$

where t_P is the actual rise time of the output pulse, t_{CVR} is the rise time of the sensor and t_I is the rise time of the instrument. From Eq. (1) a correction factor was developed to apply to the measured rise times. Rise times were calculated using the current waveform since the CVR introduced the smallest error in the measured rise time. (It should be noted that the measured rise time cannot be faster than the slowest rise time in the correction factor.)

For the output voltage pulse shown in Fig. 4 the corrected rise time is 2.1 ns.

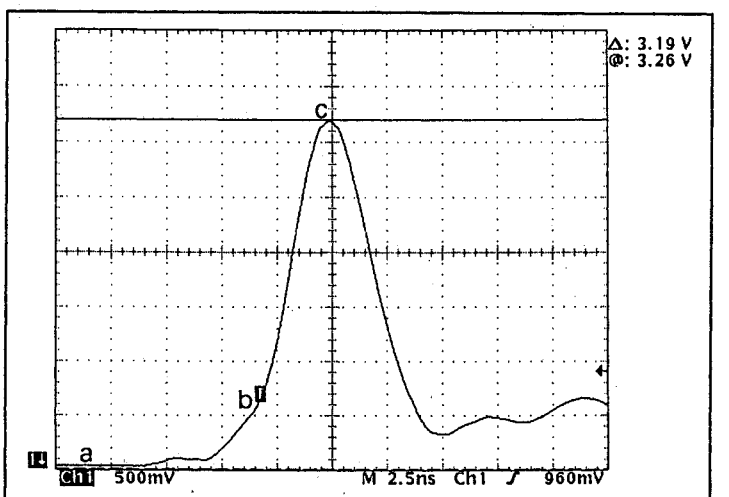

Figure 5. Fast DSRD output pulse (1V=280.2V at output). The time scale is 2.5 ns/div.

The specified t_r of the Type II DSRD is 0.5 to 1.5 ns. As noted previously, the rise time depends on the initial charge stored in the device. If the same component values are used for the Type II device a significant slow ramping period, followed by a very slow rise time will be observed. To obtain optimum performance from the Type II device, the time constant of the RLC circuit must be reduced. To reduce the period of the circuit the inductor values were kept constant and the capacitor values were changed to 2.5

nF and 5 nF for C_1 and C_2, respectively. A typical output pulse for the Type II DSRD is shown in Fig. 5. The corrected rise time is 0.74 ns.

The maximum repetition rate is determined by the main MOSFET temperature and how fast the storage capacitor C_1 can be recharged. In actual testing, MOSFET heating was a significant factor. A repetition rate of 100 kHz can be realized with this circuit but only for short periods of time. As the MOSFETs heat up their current carrying capability degrades. If the repetition rate were only limited by how fast C_1 could be charged, rates as high as 400 kHz could be obtained. In this case, the maximum realizable frequency is limited by the load resistance, the value of C_1, and the current capability and series resistance of the power supply.

Conclusion

This paper presented results obtained during testing of DSRD devices. A distinct advantage of pulse generation using this method is that the pulse amplitude is virtually unlimited. The DSRDs may be stacked in series to obtain higher amplitude pulses in the same switching rate. Obtaining higher amplitude pulses will of course require a higher initial voltage on the capacitors as well as switches capable of withstanding this voltage. High voltage power supplies are readily available but are limited to low currents. This will increase the charge time of the capacitors and thus decrease the maximum possible repetition rate. Higher breakdown voltage MOSFETs are available but the current handling capability usually decreases with increasing V_{DS}. Methods have been described[7] to effectively switch MOSFETs in series to increase the V_{DS} capability. To increase the current handling capability, the MOSFETs can also be switched in parallel.

The lifetime of these devices was observed to be in excess of 10^{10} pulses without evidence of failure. This corresponds to operating at 10 kHz continuously for 11.5 days. Lifetime is expected to be far in excess of 10^{10} pulses since the devices are not being operated in any abnormal fashion.

Future work will develop circuits used to condition or shape the pulses generated in this experiment to achieve even faster rise times with the same peak power generating capability, in particular, Silicon Avalanche Shapers (SAS) developed by the Ioffe Group will be incorporated in the circuit. Modeling efforts will be expanded to study the effects of variations in device manufacture on output performance.

Acknowledgments

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